IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1. (Currently Amended) A method comprising:

reading a first time;

storing the first time prior to entering a reduced power consumption state; and

reading a second time ~~of exiting a reduced power consumption state~~ prior to exiting the reduced power consumption state in response to an interrupt;

storing the second time ~~of exiting of the reduced power consumption state~~ in a register prior to exiting the reduced power consumption state;

after the reading and the storing the second time ~~of exiting~~, allowing an interrupt routine associated with the interrupt to execute to exit the reduced power consumption state; and

calculating a reduced power consumption state duration based on the first time and the second time ~~of exiting the reduced power consumption state~~ stored in the register.

2. (Previously Presented) The method of claim 1 wherein the reduced power consumption state is entirely responsive to the interrupt routine.

3. (Canceled).

4. (Canceled)

5. (Original) The method of claim 1 wherein the register is located in a processor.

6.-47. (Canceled)

48. (Currently Amended) An apparatus comprising:

an operating system to read a first time ~~of~~ before entering a reduced power consumption state, and

to read a second time ~~of exiting the reduced power consumption state~~ prior to exiting the reduced power consumption state in response to an interrupt; and

a main memory to store the first time ~~of entering~~, and

a register to store the second time, wherein the operating system is to allow an interrupt routine associated with the interrupt to execute to exit the reduced power consumption state after reading and storing the second time ~~of exiting~~.

49. (Previously Presented) The apparatus of claim 48 further comprising a chip to store the time of exiting the reduced power consumption state in a register.

50. (Previously Presented) The apparatus of claim 48 further comprising a processor to store the time of exciting the reduced power consumption state in a register.

51. (Previously Presented) The apparatus of claim 49 wherein the operating system further operates to perform a cycle to the chip.

52. (Previously Presented) The apparatus of claim 48 wherein the operating system further operates to calculate a reduced power consumption state duration.

53. (Previously Presented) The apparatus of claim 48 wherein the reduced power consumption state is entirely responsive to the interrupt routine.

54. (Currently Amended) An apparatus comprising:

an operating system to request a chip to store a first time ~~of~~ before entering a reduced power consumption state and a second time ~~of exiting the reduced power consumption state~~ prior to exiting the reduced power consumption state in response to an interrupt; and

the chip to store the first time ~~of entering~~ and the second time ~~of exiting the reduced power consumption state~~ in a register and to automatically calculate a reduced power consumption state duration, wherein the operating system is to allow the interrupt routine associated with the interrupt to execute to exit the reduced power consumption state after the chip stores the second time ~~of exiting~~.

55. (Previously Presented) The apparatus of claim 54 wherein the reduced power consumption state is entirely responsive to the interrupt routine.

56. (Currently Amended) An apparatus comprising:

means for reading a first time;

means for storing the first time prior to entering the reduced power consumption state in a main memory;

means for reading a second time ~~of exiting a reduced power consumption~~ prior to exiting the reduced power consumption state in response to an interrupt;

means for storing the second time ~~of~~ prior to exiting the reduced power consumption state in a register;

means for allowing the interrupt routine associated with the interrupt to execute to exit the reduced power consumption state after the reading and storing the second time ~~of exiting~~; and

means for calculating a reduced power consumption state duration based on the first time and the second time stored in the register.

57. (Canceled).

58. (Previously Presented) The apparatus of claim 56 wherein the reduced power consumption state is entirely responsive to the interrupt routine.

59. (Previously Presented) The apparatus of claim 56 wherein the register is located in a personal computer chipset.

60. (Previously Presented) The apparatus of claim 56 wherein the register is located in a processor.